IN THE CLAIMS:

Please cancel claims 7-14 without prejudice.

1. (Original) A frequency/signal converter receiving an input clock signal and generating an output signal at an output terminal, said converter comprising:

a first circuit receiving the input clock signal and generating first and second logic signals that are complementary with one another;

a loop circuit that includes a first circuit line and a second circuit line that are each coupled between a first supply voltage and a second supply voltage, the first supply voltage being greater than the second supply voltage; and

an integrator device,

wherein a current proportional to the output signal of the converter flows in the loop circuit,

the first circuit line includes a first capacitive element, and a first switch for interrupting current flow into the first capacitive element, the first switch being controlled by the first logic signal,

the second circuit line includes a second capacitive element, and a second switch for interrupting current flow into the second capacitive element, the second switch being controlled by the second logic signal, and

the first and second circuit lines are alternatively coupled to an input terminal of the integrator device in order to obtain a substantially constant voltage signal at the input terminal of the integrator device, the integrator device providing the output signal of the converter.

2. (Original) The converter according to claim 1, wherein the first and second logic signals have a period that is twice the period of the input clock signal.

3. (Original) The converter according to claim 2, wherein the first and second logic signals each has a value of logic one for one half of its period and a value of logic zero for the other half of its period.

4. (Original) The converter according to claim 1, wherein the integrator device includes:

a transconductance operational amplifier, the amplifier receiving the substantially constant voltage signal at its inverting input terminal and a reference voltage at its non-inverting terminal; and

a third capacitive element,

wherein the amplifier provides a current signal that is integrated by the third capacitive element so as to produce the output signal of the converter.

5. (Original) The converter according to claim 1,

wherein the first circuit line further includes a third switch for discharging the first capacitive element, and

the second circuit line further includes a fourth switch for discharging the second capacitive element.

6. (Original) The converter according to claim 5, wherein the third and fourth switches are controlled by pulse signals that correspond to the rising edges of the first and second logic signals.

7-14. (Canceled)

15. (Original) An integrated circuit including at least one frequency/signal converter that receives an input clock signal and generates an output signal at an output terminal, said converter comprising:

a first circuit receiving the input clock signal and generating first and second logic signals that are complementary with one another;

a loop circuit that includes a first circuit line and a second circuit line that are each coupled between a first supply voltage and a second supply voltage, the first supply voltage being greater than the second supply voltage; and

an integrator device,

wherein a current proportional to the output signal of the converter flows in the loop circuit,

the first circuit line includes a first capacitive element, and a first switch for interrupting current flow into the first capacitive element, the first switch being controlled by the first logic signal,

the second circuit line includes a second capacitive element, and a second switch for interrupting current flow into the second capacitive element, the second switch being controlled by the second logic signal, and

the first and second circuit lines are alternatively coupled to an input terminal of the integrator device in order to obtain a substantially constant voltage signal at the input terminal of the integrator device, the integrator device providing the output signal of the converter.

16. (Original) The integrated circuit according to claim 15, wherein the first and second logic signals have a period that is twice the period of the input clock signal.

17. (Original) The integrated circuit according to claim 16, wherein the first and second logic signals each has a value of logic one for one half of its period and a value of logic zero for the other half of its period.

18. (Original) The integrated circuit according to claim 15, wherein the integrator device includes:

a transconductance operational amplifier, the amplifier receiving the substantially constant voltage signal at its inverting input terminal and a reference voltage at its non-inverting terminal; and

a third capacitive element,

wherein the amplifier provides a current signal that is integrated by the third capacitive element so as to produce the output signal of the converter.

19. (Original) The integrated circuit according to claim 15,

wherein the first circuit line further includes a third switch for discharging the first capacitive element,

the second circuit line further includes a fourth switch for discharging the second capacitive element, and

the third and fourth switches are controlled by pulse signals that correspond to the rising edges of the first and second logic signals.